Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A phase lock loop comprising a charge pump fabricated on a substrate ~~for use in a phase lock loop system~~, the charge pump comprising:

a first input stage having a first input transistor that receives a first control signal, a first complementary transistor, and a first discharging transistor,

where the drain terminals of the first input transistor and the first complementary transistor are ~~and the drain terminals~~ connected with a source terminal of the first discharging transistor, and the first complementary transistor is operable to receive a first reference signal;

a second input stage having a second switching transistor that receives a second control signal, a second complementary transistor, and a second discharging transistor,

where the drain terminals of the second input transistor and the second complementary transistor are ~~and the drain terminals~~ connected with a source terminal of the second discharging transistor, and the second complementary transistor operable to receive a second reference signal; and

first and second output nodes for transmitting ~~a differential pair~~ output signals, the first and second output nodes being coupled to ~~connected with~~ the first and second complementary transistors, respectively.

2. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1, where the charge pump is operable to receive the first and second reference signals from a voltage divider circuit.

3. (Currently Amended) The phase lock look ~~charge pump~~ of claim 2, where the first and second reference signals are substantially the same.

4. (Currently Amended) The phase lock look ~~charge pump~~ of claim 3, where the reference signals are substantially half the supply voltage.

5. (Currently Amended) The phase lock look ~~charge pump~~ of claim 2, where the voltage divider circuit comprise a plurality of interdigitized resistors.

6. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1, where the first and second reference signals are received from first and second voltage divider circuits.

7. (Currently Amended) The phase lock look ~~charge pump~~ of claim 6, where the first and second reference signals are substantially the same.

8. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1, where the first reference signal includes a constant voltage level that is between minimum and maximum voltage levels of the first input signal.

9. (Currently Amended) The phase lock look ~~charge pump~~ of claim 8, where the first reference signal includes a constant voltage level that is substantially equal to a midpoint of a voltage range of the first input signal.

10. (Currently Amended) The phase lock look ~~charge pump~~ of claim 8, where the first complementary transistor switches on substantially when the first input transistor switches off and the first complementary transistor switches off substantially when the first input transistor switches on.

11. (Currently Amended) The phase lock look ~~charge pump~~ of claim 10, where the second complementary transistor-switches on substantially when the second

input transistor switches off and the second complementary transistor switches off substantially when the second input transistor switches on.

12. (Canceled)

13. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1 further comprising a biasing circuit that provides a biasing signal to gate terminals of the first and second discharging transistors.

14. (Currently Amended) The phase lock look ~~charge pump~~ of claim 13 wherein one of the first and second output nodes connects with a filter that reduces coupled switching noise at an output node of the filter.

15. (Currently Amended) The phase lock look ~~charge pump~~ of claim 14, where the filter comprises a transistor based filter.

16. (Currently Amended) The phase lock look ~~charge pump~~ of claim 15, where a filter output connects with the voltage-to-current converter.

17. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1, where the first and second input transistors comprise switching transistors.

18. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1 further comprising a first charging transistor connected between a supply voltage and the first input transistor and a second charging transistor connected between a supply voltage and the second input transistor.

19. (Currently Amended) The phase lock look ~~charge pump~~ of claim 18 further comprising a third charging transistor connected between the supply voltage and

the first complementary transistor and a fourth charging transistor connected between the supply voltage and the second complementary transistor.

20. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1, where the charge pump operates with a supply voltage of less than 2.5 volts.

21. (Currently Amended) The phase lock look ~~charge pump~~ of claim 20, where the charge pump operates with a supply voltage of less than 1.9 volts.

22. (Currently Amended) The phase lock look ~~charge pump~~ of claim 20, where the charge pump has at most three transistors connected via source and drain terminals between the supply voltage and ground.

23. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1, where the signals at the first and second output nodes are substantially isolated from signal noise in the first and second control ~~UP and DW~~ signals.

24. (Currently Amended) The phase lock look ~~charge pump~~ of claim 23, where the signals at the first and second output nodes are substantially isolated from switching noise caused by the first and second input transistors.

25. (Currently Amended) The phase lock look ~~charge pump~~ of claim 1 further comprising:

first and second charging transistors connected between a supply voltage and the first and second input transistors, respectively;

a voltage divider circuit that provides a reference signal to gate terminals of the first and second complementary transistors, where the reference signal is substantially half the supply voltage;

third and fourth charging transistors connected between the supply voltage and the first and second complementary transistor, respectively;

a biasing circuit that provides a biasing signal to gate terminals of the first and second discharging transistors; and

a filter comprising transistors operable to reduce coupled switching noise at an output node of the filter;

where the first complementary transistor switches on substantially when the first input transistor switches off and the first complementary transistor switches off substantially when the first input transistor switches on.

26. (Currently Amended) ~~A~~The phase lock loop circuit of claim 25, further comprising a phase and frequency detector connected with the charge pump ~~of claim 25~~, ~~a voltage-to-current converter and~~ a loop filter connected with the charge pump, and a ~~the~~ voltage-to-current converter coupled between the loop filter and ~~being connected with~~ a current controlled oscillator that is connected with the phase and frequency detector.

27. (Currently Amended) ~~A~~The phase lock loop circuit of claim 26, where the voltage-to-current converter receives a differential signal from the charge pump and transmits a non-differential signal to the loop filter.

28. (Original) A method of pumping a charge in a semiconductor based charge pump for use in a phase lock loop circuit, comprising:

receiving first and second input signals at first and second switching transistors;

providing a biasing signal to first and second complementary transistors such that the complementary transistors change states between off and on substantially complementary to the state of the respective first and second switching transistors; and

generating a first output signal from at least one of the first and second complementary transistors.

29. (Currently Amended) The method of claim 28, further comprising providing a second output signal from the other of the at least ~~feast~~ one of the first and second complementary transistors, where the first and second output signals form a differential pair.

30. (Original) A differential charge pump for use in a phase lock loop, comprising:

a first transistor pair, comprising a first switching transistor and a first complementary transistor;

a first switching transistor gate, associated with the first switching transistor, coupled to a first control signal, and a first complementary transistor gate, associated with the first complementary transistor, being coupled to a constant bias voltage such that the first complementary transistor is indirectly controlled by the first control signal;

a second transistor pair, comprising a second switching transistor and a second complementary transistor; and

a second switching transistor gate, associated with the second switching transistor, coupled to a second control signal, and a second complementary transistor gate, associated with the second complementary transistor, being coupled to the constant bias voltage such that the second complementary transistor is indirectly controlled by the second control signal.

31. (Original) The differential charge pump of claim 30, further comprising: a second transistor pair, comprising a second switching transistor and a second complementary transistor; and

a second switching transistor gate, associated with the second switching transistor, coupled to a second control signal, and a second complementary transistor gate, associated with the second complementary transistor, being coupled to a constant bias voltage such that the first complementary transistor is indirectly controlled by the first control signal.

32. (Original) The differential charge pump of claim 30, wherein the first switching transistor is coupled between a first current source and a first current sink.

33. (Original) The differential charge pump of claim 32, wherein the first complementary transistor is coupled between a first cascode transistor pair and the first current sink.

34. (Original) The differential charge pump of claim 33, wherein the first cascode transistor pair is coupled to a supply voltage.

35. (Original) The differential charge pump of claim 34, wherein the first bias voltage is less than the supply voltage.

36. (Original) The differential charge pump of claim 34, wherein the first bias voltage is approximately half of the supply voltage.

37. (Original) The differential charge pump of claim 34, wherein the supply voltage is approximately 3 Volts and the first bias voltage is approximately 1.5 Volts.

38. (Original) The differential charge pump of claim 30, wherein the indirect control of the first complementary transistor by the first control voltage reduces switching noise in the differential charge pump.

Amendments to the Drawings

In the Drawings:

Please replace drawing sheets 1-5 (showing Figs. 1-5) with the newly-submitted figures attached herewith on separate sheets.

Figure 3 has been replaced with Figures 3A and 3B (Sheets 3 and 4, respectively), Figure 3B showing a second voltage divider circuit, with a second bias voltage.

Figure 4 (Sheet 5) has been amended to correct a stray line between transistor 444 and Ico, and a stray line between ground and transistor 446.

Attachment: Replacement Sheets